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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,016	07/23/2003	Manish Sharma	200207743-1	8424

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,016	SHARMA ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-19,21-25 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-19,21-23 and 28* is/are rejected.

7)☒ Claim(s) *24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 7, 8, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis (US 2002/0087886) in view of Cloud et al (6,498,739 hereinafter "Cloud").

Ellis teaches an integrated microchip (Fig. 10C and par 107) comprising a non-volatile memory (MRAM 88); a DRAM (66); a graphics cart (82); video processing card (86); a DSP (89); a master processor unit (93) and a plurality of slave processors in parallel or multitasking processing (94), each processor being integrated with the MRAM and DRAM memory (par 107) and accessing data from a corresponding MRAM and DRAM memory that is integrated with the processor element, and performing processing on the data (par 107). However, Ellis fails to explicitly teach the MRAM and DRAM memories are integrated in a shared memory cell and each shared memory cell comprising a single MRAM cell and a single DRAM cell. This is what Cloud teaches (Fig. 8). Cloud teaches a shadow RAM cell (Fig. 8, 800) includes a DRAM cell (801) coupled to a non-volatile memory cell (803) which can be a MRAM cell as suggest by Ellis. It would have been obvious to one of ordinary skill in the art at the time the

present invention was made to combine the teachings of single shared memory cell includes MRAM cell and DRAM cell of Cloud into the integrated system of Ellis in order to permit the slow access times to the MRAM cell to be compensated for, since all of the data which is repeatedly read or written is kept for as long as possible in the additional, fast DRAM cell. It is only during the permanent saving of data, for example, the data is then transferred into the MRAM cell, which permits great flexibility in the range of application. Therefore, at least claims 1, 2, 4, 7 and 8 would have been obvious by Ellis and Cloud.

As per claim 3, Ellis teaches each processor element can access a plurality of non-volatile memory cells (par 107, in parallel or multitask processing or in network).

Claim 22 is similar in scope to claim 1, and thus is rejected under similar rationale.

Claim 23 is similar in scope to claim 1, and additionally requires a CPU (inherent by any computer system to include the CPU in order to function properly, such as, master control unit 93).

3. Claims 9-19, 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis (US 2002/0087886) and Cloud et al (6,498,739 hereinafter "Cloud") in view of Young (5,621,683).

The teachings of Ellis and Cloud are given in previous paragraph of this Office action. However, Ellis and Cloud fail to explicitly suggest or teach an array of image sensors and an image sensor corresponding with each of the magnetic memory cells. This is what Young teaches (col. 1, lines 6-18). It would have been obvious to one of

ordinary skill in the art at the time the present invention was made to combine the teachings of image sensor of Young into the memory substrate of Ellis because this is what Young teaches (see col. 1, lines 6-18). Therefore, at claims 9 and 28 would have been obvious.

As per claim 10, Young teaches each image sensor receives image data that can be stored in a corresponding non-volatile memory element (title).

As per claim 11, Ellis teaches each processing element performs processing on the image data stored in a corresponding non-volatile memory element (Fig. 10C, MRAM 88).

As per claim 12, Ellis teaches received image data is additionally stored in at least one DRAM cell (66) corresponding with the non-volatile memory element (88).

As per claim 13, Young teaches each image sensor (col. 1, lines 6-18) is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element (Ellis, 115) formed adjacent to a non-volatile memory element.

As per claim 14, Young teaches each image sensor (col. 1, lines 6-18) is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element (Ellis, 94) and DRAM cell (66) formed adjacent to a non-volatile memory element (88).

As per claim 15, the combined system fails to explicitly teach an array of display pixels, a display pixel corresponding with at least one of the non-volatile memory cells. However, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of the combined system as claimed because an image comprises a plurality of display pixels is well known and well use in the art.

As per claim 16, Ellis teaches each display pixel displays image data that is stored in a corresponding non-volatile memory element (88).

As per claim 17, Ellis teaches each processing element (94) performs processing on the image data stored in a corresponding non-volatile memory element (88).

As per claim 18, Ellis teaches the received image data is additionally stored in at least one DRAM cell (66) corresponding with the non-volatile memory element.

As per claim 19, Ellis teaches at least one display pixel receives image data from a plurality of non-volatile memory elements (88).

As per claim 21, Ellis teaches each display pixel is formed adjacent to a corresponding non-volatile memory element (88), and is formed adjacent to a substrate comprising a corresponding processor element (94) and DRAM cell (66) formed adjacent to the non-volatile memory element.

Allowable Subject Matter

4. Claims 24 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671